BCA-III			
COMPUTER ARCHITECTURE (203)			
S.NO.	NAME	ENROLL.NO.	TOPICS
1	CHINMOY SAREN	00290102018	Register Transfer
2	DEEPANSHU YADAV	00390102018	Micro Operation
3	DEVAYANI R	00490102018	Register Transfer Language
4	DHRUV UTTAM	00590102018	Bus Transfer
5	HARSH BHARDWAJ	00690102018	Memory Transfer
6	HIMANSHU JAGYA	00790102018	Arthmetic Micro Operation
7	JASKARAN SINGH	00890102018	Logic Micro Operation
8	JASPREET KAUR	00990102018	Shift Microoperation
9	JEEVANDEEP SAINI	01090102018	Arthmatic Logic Shift Microperation
10	KALPESH GUPTA	01190102018	Instruction Codes
11	KARTIK TANWAR	01290102018	Computer Register
12	MANTHAN RANA	01390102018	Computer Instruction
13	NAVNEET KUMAR	01490102018	Register Reference Instruction
14	PANKAJ KHANDELWAL	01590102018	Input Instruction
15	PRERNA KUMARI	01690102018	Output Instruction
16	PRIYA	01790102018	Design Of Accumulator Logic
17	SARTHAK NAGPAL	01990102018	Design Of Control Unit
18	SHUBHAM TIWARI	02090102018	General Register Organisation
19	SOURAV CHAUHAN	02190102018	Stack Organisation
20	SHRESTH KHANDURI	35390102018	Instruction Format
21	YOGESH SINGH	35490102018	Addressing Modes
22	AKASH SHARMA	35690102018	Risc
23	RUDRA NARAYANA JENA	40290102018	Cisc
24	SUVISHA S	40490102018	Differentiate Between Risc & Cisc
25	AMAN SINGH	40590102018	Pipeline Processing

26	NAVNEET SHOKEEN	40690102018	Vector Processing
27	ROHIT SINGH	40790102018	Arithmatic Pipeline Instruction
28	MANPREET SINGH	41090102018	Vector Operation
29	SUNNY KATARIA	41190102018	Matrix Multiplication
30	SHIVANI GUPTA	41390102018	Memory Interleaving
31	DHRUV MALHOTRA	41590102018	Multiplication Algorithm
32	BHASKAR AGGARWAL	41690102018	Multiplication Algorithm Implementation Using One Suitable Example
33	ABHISHEK	41890102018	Division Algorithm
34	NEHA ARORA	41990102018	Division Algorithm Implementation Using One Suitable Example
35	ABHINAV RANA	42090102018	Fixed Point Implementation Of Division Algorithm
36	SAKSHAM	42390102018	Peripheral Devices
37	BHAVYA MALHOTRA	42490102018	Input Interfaces
38	AVINASH JAKHAR	42590102018	Output Interface
39	DEEPAK UPRETI	42690102018	Asynchronous Data Transfer
40	RAVINDER SHAH	42790102018	Mode Of Transfer
41	PRABHNOOR SINGH	42890102018	Priority Interrupt
42	SHIVAM ARORA	42990102018	Direct Memory Access
43	ASHISH THAKUR	43290102018	Memory Hierarchy
44	ASHWIN SABBANI	43390102018	Main Memory
45	ANUBHAV SINGH NEGI	00151402018	Auxiliary Memory
46	ARUNA JOSHI	00251402018	Associative Memory
47	AYUSH RAWAT	00351402018	Cache Memory
48	CHIRAG	00451402018	Virtual Memory
49	DEEP ANAND	00551402018	Memory Management Hardware
50	DINESH DADWAL	00651402018	Register Transfer
51	HITESH BANSAL	00751402018	Micro Operation
52	LAKSHAY GUPTA	00851402018	Register Transfer Language

53	MEHUL SHRIVASTAVA	00951402018	Bus Transfer
54	RISHABH SINGH	01051402018	Memory Transfer
55	RIYA WADHWA	01151402018	Arthmetic Micro Operation
56	SHUBHAM TRIPATHI	01251402018	Logic Micro Operation
57	ZUBER ALAM	01351402018	Shift Microoperation
58	JANESH KUMAR RAI	40251402018	Arthmatic Logic Shift Microperation
59	NIKHIL PRAJAPATI	40351402018	Instruction Codes
60	SAHIL LUCKY SAINI	40551402018	Computer Register
61	SOJIN GEORGE	01751402017	Computer Instruction