| BCA- 3RD SEM | | | | | | |
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| COMPUTER ARCHITECTURE (203) - MCQS | | | | | | |
| **S.NO** | **QUESTIONS** | **A** | **B** | **C** | **D** | **ANS** |
| **1** | RTL stands for: | Random transfer language | Register transfer language | Arithmetic transfer language | All of these | **B** |
| **2** | Which operations are used for addition, subtraction, increment, decrement and complement function: | Bus | Memory transfer | Arithmetic operation | All of these | **D** |
| **3** | The method of writing symbol to indicate a provided computational process is called as a: | Programming language | Random transfer language | Register transfer language | Arithmetic transfer language | **A** |
| **4** | Which language is termed as the symbolic depiction used for indicating the series: | Random transfer language | Register transfer language | Arithmetic transfer language | All of these | **B** |
| **5** | The register that includes the address of the memory unit is termed as the : | MAR | PC | IR | None of these | **A** |
| **6** | In register transfer the processor register as: | MAR | PC | IR | RI | **D** |
| **7** | How many types of micro operations: | 2 | 4 | 6 | 8 | **B** |
| **8** | Which are the operation that a computer performs on data that put in register: | Register transfer | Arithmetic | Logical | All of these | **D** |
| **9** | In memory read the operation puts memory address on to a register known as : | PC | ALU | MR | All of these | **C** |
| **10** | Which operation puts memory address in memory address register and data in DR: | Memory read | Memory Write | Both | None | **B** |
| **11** | In the following indexed addressing mode instruction, MOV 5(R1), LOC the effective address is _____ | EA = 5+R1 | EA = R1 | EA = [R1] | EA = 5+[R1] | **D** |
| **12** | The addressing mode which makes use of in-direction pointers is _____ | Indirect addressing mode | Index addressing mode | Relative addressing mode | Offset addressing mode | **A** |
| **13** | _____ addressing mode is most suitable to change the normal sequence of execution of instructions. | Relative | Indirect | Index with Offset | Immediate | **A** |
| **14** | The effective address of the following instruction is MUL 5(R1,R2). | 5+R1+R2 | 5+(R1*R2) | 5+[R1]+[R2] | 5*([R1]+[R2]) | **C** |
| **15** | The addressing mode, where you directly specify the operand value is _____ | Immediate | Direct | Definite | Relative | **A** |
| **16** | Which of the following register is used in the control unit of the CPU to indicate the next instruction which is to be executed ? | Accumulator | Index register | Instruction decoder | Program counter | **D** |

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| **17** | If a processor does not have any stack pointer register, then | It cannot have subroutine call instruction | It can have subroutine call instruction, but no nested subroutine | Nested subroutine calls are possible, but interrupts are not | All sequences of subroutine calls and also interrupts are | **D** |
| **18** | The Sun micro systems processors usually follow _____ architecture | CISC | ISA | ULTRA SPARC | RISC | **D** |
| **19** | Which of the architecture is power efficient? | CISC | RISC | ISA | IANA | **B** |
| **20** | The master indicates that the address is loaded onto the BUS, by activating _____ signal. | MSYN | SSYN | WMFC | INTR | **A** |
| **21** | In IBM's S360/370 systems _____ lines are used to select the I/O devices | SCAN in and out | Connect | Search | Peripheral | **A** |
| **22** | The transmission on the asynchronous BUS is also called _____ | Switch mode transmission | Variable transfer | Bulk transfer | Hand-Shake transmission | **D** |
| **23** | The BUS that allows I/O, memory and Processor to coexist is _____ | Attributed BUS | Processor BUS | Backplane BUS | External BUS | **C** |
| **24** | The chip can be disabled or cut off from an external connection using _____ | Chip select | LOCK | ACPT | RESET | **A** |
| **25** | The less space consideration as lead to the development of _____ (for large memories). | SIMM's | DIMS's | SRAM's | Both SIMM's and DIMS's | **D** |
| **26** | The reason for the implementation of the cache memory is _____ | To increase the internal memory of the system | The difference in speeds of operation of the processor and memory | To reduce the memory access and cycle time | All of the mentioned | **B** |
| **27** | The correspondence between the main memory blocks and those in the cache is given by _____ | Hash function | Mapping function | Locale function | Assign function | **B** |
| **28** | The approach where the memory contents are transferred directly to the processor from the memory is called _____ | Read-later | Read-through | Early-start | None of the mentioned | **C** |
| **29** | The algorithm to remove and place new contents into the cache is called _____ | Replacement algorithm | Renewal algorithm | Updation | None of the mentioned | **A** |
| **30** | Consider a memory organised into 8K rows, and that it takes 4 cycles to complete a read operation. Then the refresh overhead of the chip is _____ | 0.0021 | 0.0038 | 0.0064 | 0.0128 | **B** |

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| **31** | What is memory hierarchy ? | | | | | |
| **32** | Give difference between RISC and CISC. | | | | | |
| **33** | What is asynchronous data transfer? Explain some methods? | | | | | |
| **34** | Differenciate between main memory & Auxiliary Memory | | | | | |
| **35** | Explain computer Registers | | | | | |